DESIGN OF AN LTCC INTEGRATED TRI-BAND DIRECT CONVERSION RECEIVER FRONT-END MODULE

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Abstract—**This paper presents the results of a front-end receiver module integrating GSM/DCS/PCS band select functions and a direct conversion IC on a low temperature co-fired ceramic (LTCC) substrate. The front-end-module (FEM) integrated a SP3T GaAs PHEMT switch for band selection, three SAW filters for pre-selection, and a direct conversion IC for down conversion of the RF signal. Integrated passives included a PCS balun, direct conversion IC matching elements and structures to improve the performance of differential SAW filters. The LTCC module contained 24 embedded passives and 15 surface mount components integrated on a 328 mil x 586 mil, 19-layer multi-layer integrated circuit (MLIC). Receiver Sensitivity was better than –114 dBm, the system Noise Figure was less than 9 dB, and the Return Loss characteristics measured at the antenna input port were better than 10 dB for all three bands. EM simulation was used to achieve first pass design success and the modeling approach yielded excellent agreement between measured and simulated results.**

I. INTRODUCTION

The advent of several emerging technologies has enabled the development of high performance, multi-mission, handheld software defined radio (SDR). One of the basic building blocks in the SDR architecture is a multi-band analog RF section. This paper focuses on the design, fabrication, and characterization of a miniature, low power, multi-band implementation of the receiver front-end block.

Several key technologies were brought together in the front-end module: GaAs PHEMT switches, Surface Acoustic Wave (SAW) filters, direct conversion receiver architecture (Motorola IC), and a multi-layer ceramic substrate with integrated passive components. Attributes of the LTCC, which made it attractive as an integration platform included cavity formation to support SAW filter hermiticity, vertical integration for DC interconnect and RF passive structure definition, and low loss stripline design to reduce I^2 R losses in the sections prior to the direct conversion IC, which directly affected the noise figure of the receiver. Key factors influencing the design of the FEM included: the use of a direct conversion IC requiring differential input signals, the availability and characteristics of SAW filters with dual ended outputs, and the decision to use the direct conversion IC packaged with a ball grid array (BGA) interposer. Although a bit larger in size than a module utilizing a direct chip attach (DCA) version of the direct conversion IC, this module mitigated the yield risk due to known good die (KGD) by using pre-tested BGA versions of the direct conversion IC.

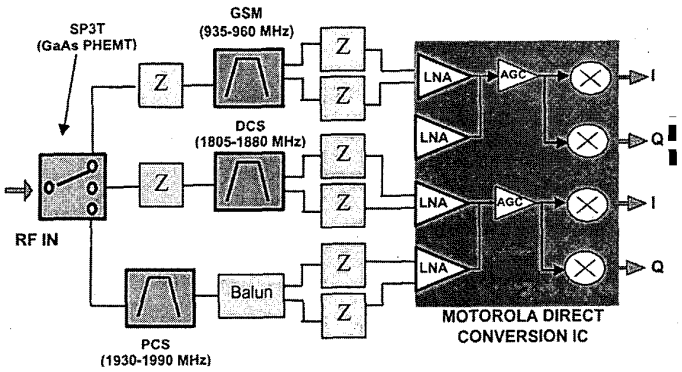

Figure 1: Block diagram of the integrated Front-End Module. Impedance matches and the balun were integrated using LTCC.

II. FILTER CHARACTERISTICS

The filter slots noted in the overall block diagram shown in Figure 1 determined the frequency bands of operation. In order to achieve a reasonably compact module, surface acoustic wave (SAW) and bulk acoustic wave (BAW) technologies were the preferred choices. However, the large number of SAW vendors which have developed components for the various cellular bands and the fact that the BAW suppliers seem to lag behind the SAW in developing a cellular filter portfolio, drove the decision to select an all-SAW design for the prototype presented in this work.

A special LTCC test module was designed and fabricated which enabled evaluation the SAW die S-parameters in a physical environment, which closely emulated the environment of the final Integrated RF module design. Shown in Figure 2 is a top view of the special test module with the EGSM SAW die in place and showing the wire bonds required to achieve electrical connections. Equivalent circuits representing the RF probe pads, internal vias, and traces up to the wire bond pads were determined from s-parameter characterization of the test module and used to de-embed the filter s-parameters for use in RF circuit simulation.

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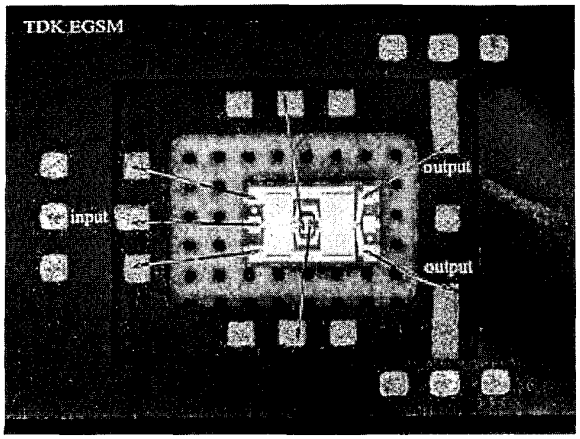


Figure 2: Photograph showing the EGSM SAW filter assembled in a special evaluation test module.

The process was repeated for the DCS and PCS SAW filters which were configured to optimally drive the Motorola direct conversion IC. The amplitude balance measured for the DCS filter exceeded 1 dB peak-to-peak over most of the band and reached a maximum value of 3.3 dB. However, the effect of this amplitude error on the Integrated RF module performance in the DCS band was negligible. The phase balance was less than 20 degrees peak-to-peak over 97% of the band and also did not impact receiver performance. The amplitude balance for the GSM filter was 2 dB peak-to-peak worst cases and the phase balance was 11 degrees peak-to-peak worst case. Again, the phase and amplitude imbalance characteristics proved adequate for this application.

III. LTCC DESIGN

The schematics outlining the matching networks used in the module are shown in Figure 3. A balun is detailed for the 1900 MHz (PCS) filter to accommodate the unbalanced output, immediately after the balun are series C, shunt L networks for matching to the direct conversion IC. A shunt C, series L combination was used at the input of the single-ended 1800 MHz (DCS) SAW filter in order to improve the filter's Return Loss characteristics. Series L, shunt C networks were used on each leg of the DCS filter's balanced output in order to improve phase and amplitude balance followed by a series L to provide a match to the direct conversion IC. Similarly, a series L, shunt C combination was used at the input of the single-ended 900 MHz (EGSM) SAW filter for Return Loss improvement and series C, shunt L networks were used on each leg of the GSM filter's balanced output to provide a match to the direct conversion IC.

In order to accurately design impedance matching networks for the direct conversion IC, the input impedance at the die level to each LNA was rotated from the known values to the reference plane defined by the BGA/LTCC interface.

A model of the package was required in order to transform the die level impedance and was derived from material specifications and mechanical drawings for the interposer obtained from the manufacturer. Said specifications were used to generate a physical model for electromagnetic

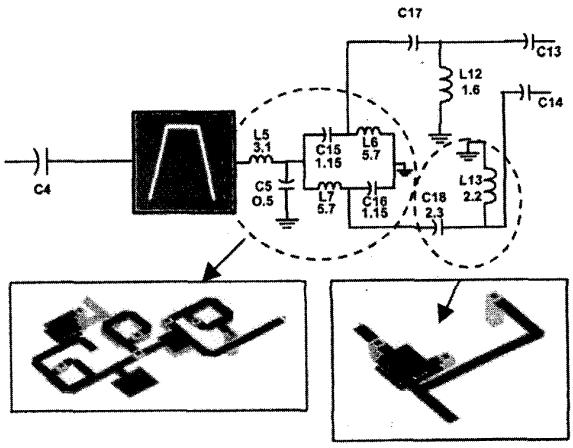


Figure 3-a: PCS balun and impedance matching schematic. The corresponding realization of the lumped elements in the LTCC is also shown with the exception of C17 and L12, which are similar to the series C, and shunt L matching elements shown.

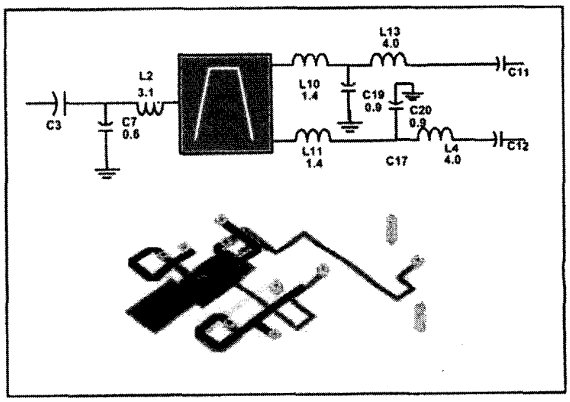
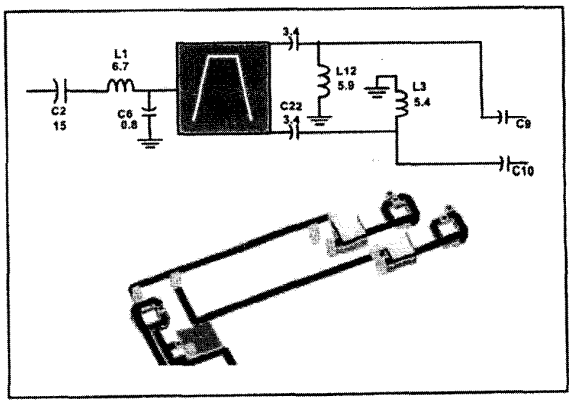


Figure 3-b and 3-c (below): DCS and GSM (below) impedance matching schematic and the corresponding realization of the lumped elements in the LTCC.



simulation of the package ports of interest. The 3-D model

generated using the SONNET *em* simulator is shown in Figure 4.

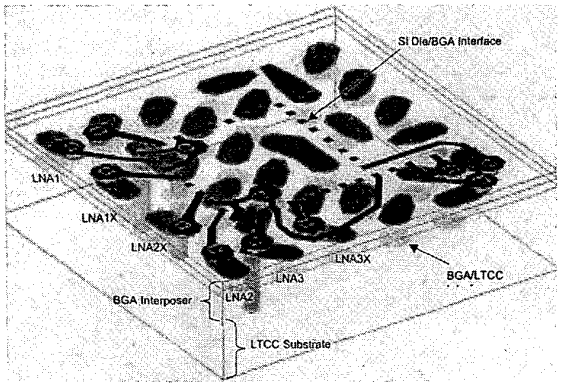


Figure 4: Interposer model used to transform die level impedance to BGA/LTCC interface.

The overall size and layer structure of the integrated module was a direct result of the surface mount components used in the design. The size of the module was mostly influenced most by the size of the direct conversion IC BGA (200 x 200 mils) and the module thickness (70.3 mils) was defined to be twice as thick as the deepest cavity used. Hence, nineteen layers of 3.7-mil thick Dupont 951 ceramic (ε_r =7.8, tand =0.002) were used in the module. The R.F. performance of the SAW filters dictated the use of a ground plane beneath the die, which also served as the top-level ground plane for the embedded stripline components. Hence, the integrated module was divided into two regions, the top half contained the SAW filters and provided a place to rout all DC control lines and the bottom half contained the RF embedded passives/transmission lines. This scheme, shown pictorially in schematic cross section in Figure 5, also provided excellent shielding for the RF components from potential noise sources present on the DC control lines. Shown in Figure 6 is the complete LTCC layout for all RF components used in the module. The imbedded ground plane was removed from the plot for clarity. Figure 7 shows the final module assembly. The generous cavity dimensions used to house the SAW filter die were designed to replicate packaged SAW devices on hand and were not optimized for size. DC blocking capacitors (0402) were used at the RF inputs to the FET switch and direct conversion IC.

IV. Measured and Simulated Results

Characterization focused on quantifying integrated module receiver performance and the corresponding effects of LTCC fabrication. In order to address the latter, subassemblies consisting of the SAW device and the corresponding matching elements were generated for each band. The subassemblies were designed for RF probe using the integrated module database and fabricated along with the full module to eliminate the effects of lot variation. Several interesting observations were made during the characterization and subsequent of analysis of the subassemblies. The data in Figure 8 shows the transmission characteristics measured from the EGSM input-matching network, through the SAW filter and the conversion IC

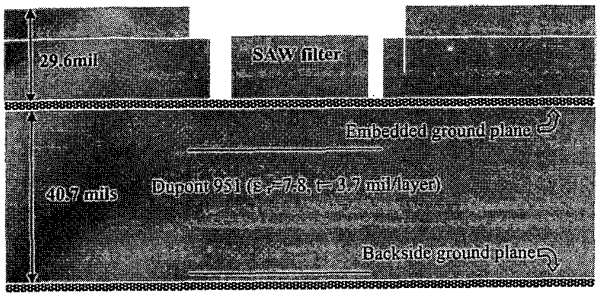


Figure 5: Integrated module schematic cross-section.

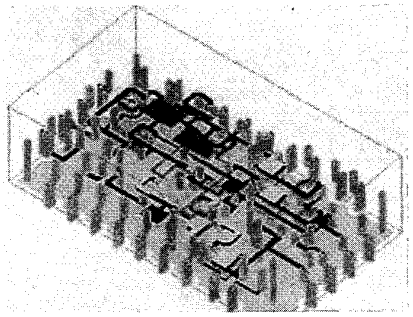


Figure 6: LTCC layout showing the integrated passives used to support the RF functions.

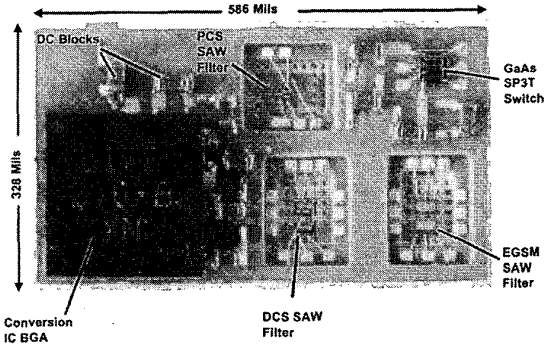


Figure 7: Final assembly for the completed integrated module.

matching structure. Through RF measurements of the subassembly and modeling, capacitive coupling between the input SAW match and one of the legs of the output match that degraded the stopband performance of the filter was identified.

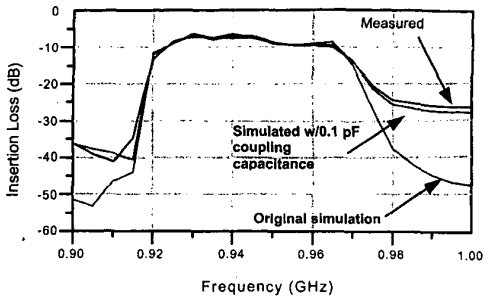


Figure 8: GSM sub-assembly passband response.

Hence, as the vertical integration capability of the LTCC is utilized, EM simulation of individual structures must be augmented with a rigorous coupling analysis. Another important aspect of the subassembly analysis was identification of the I^2*R losses associated with the receiver sections prior to the conversion IC since these losses directly added to the noise figure of the system. Table 1 summarizes the I^2*R losses for the integrated module.

Band	Switch Loss (dB	Filter + Match (dB)	Total Loss (dB)
GSM	0.7	2.3	3
DCS	1.2	2.5	3.7
PCS	1.5	1.6	3.1

Table 1: Summary of the mid-band I^2*R losses measured prior to the conversion IC LNA input for the integrated module.

The effects of LTCC metalization thickness (0.6 mil simulated, 1 mil actual) on the performance of the module are shown in Figure 9 for the DCS band; similar effects were noted in the other two bands. Figure 9 plots data obtained from an extension made to the 2.5D Sonnet simulator in order to account for metal thickness, which,

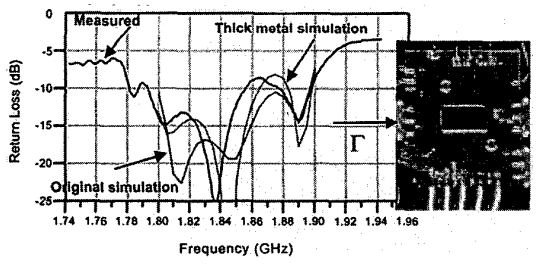


Figure 9: DCS Return Loss characteristics measured at the module antenna port and the corresponding simulations.

was required in order to accurately predict Return Loss. The accuracy in the Return Loss prediction validated the interposer model since the conjugate match designed was based on die level impedance data. Table 2 summarizes the integrated RF module receiver performance, which met all applicable performance goals. The general test approach was to operate the module as a direct conversion receiver front end.

Test	950 MHz	1870 MHz	1950 MHz
Noise Figure[1]	8 dB	8.5 dB	8 dB
Sensitivity[2] (140 KHz B.W.)	-114 dBm	-114 dBm	-114 dBm
Return Loss	18 dB	11 dB	15 dB
Conversion Gain	23 dB	20 dB	22 dB
Side Band Suppression	46 dB	41 dB	32 dB
Switch Isolation	23 dB	19 dB	18 dB
Selectivity	48 dB at 910 MHz 28 db at 990 MHz	23 dB at 1750 MHz 14 db at 1950 MHz	31 dB at 1850 MHz 28 db at 2050 MHz
Supply Current	43 mA	45 mA	44 mA

Note 1: measured using an Ailtech 15 db ENR noise source.
Note 2: Measured using twice power signal generator method.

Table 2: Summary of measured integrated receiver data.

V. Summary

A complete high performance, multi-band, direct conversion receiver front end consisting of an RF band select switch, RF pre-selector filters, low noise amplifiers, quadrature mixers, integral voltage controlled oscillators, and integral automatic gain control has been demonstrated. Some variation in the values of noise figure and input return loss compared to expected theoretical values were noted. However, these differences were considered minor for such a unique, high performance, receiver front end of this type. Subassemblies were used to identify coupling and metal thickness effects on module performance. An extension to the EM simulator was made to account for metal thickness effects and the model derived for the packaged direct conversion IC was verified.

VI. Acknowledgements

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